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PG semester III

Unit :- 5

Topic - ripple counter

Ripple (Asynchronous) Counters

A counter can be described as a tallying device that tallies, or counts some number of events. An electronic counter needs that the data be converted into electric pulses, each of which represent one bit of information, or one happening. These pulses are introduced at the input and the counter tallies each

and every one keeping a cumulative total.

(A) 4- bit Ripple Counter:- When several flip flops are connected together in a certain way, they form a counting chain that is capable of actually counting or tallying the events.

Consider four interconnected T- type flip flops as shown in fig (1)(a). The pulses to be counted are applied to the first flip-flop. The negative-going pulses have been considered.

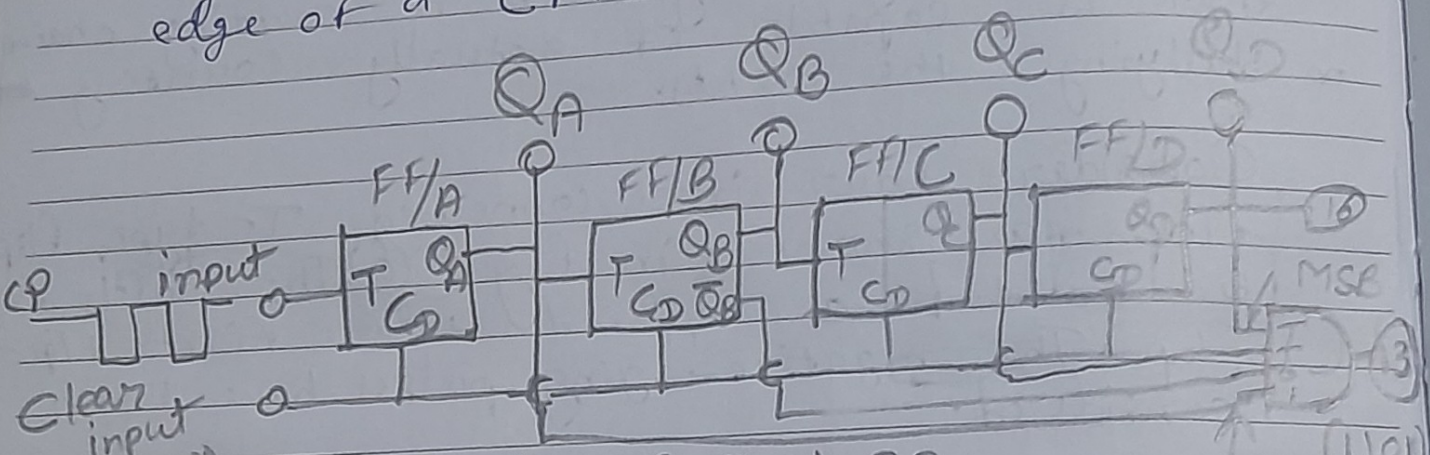
For a T- type binary, it may be remembered that:

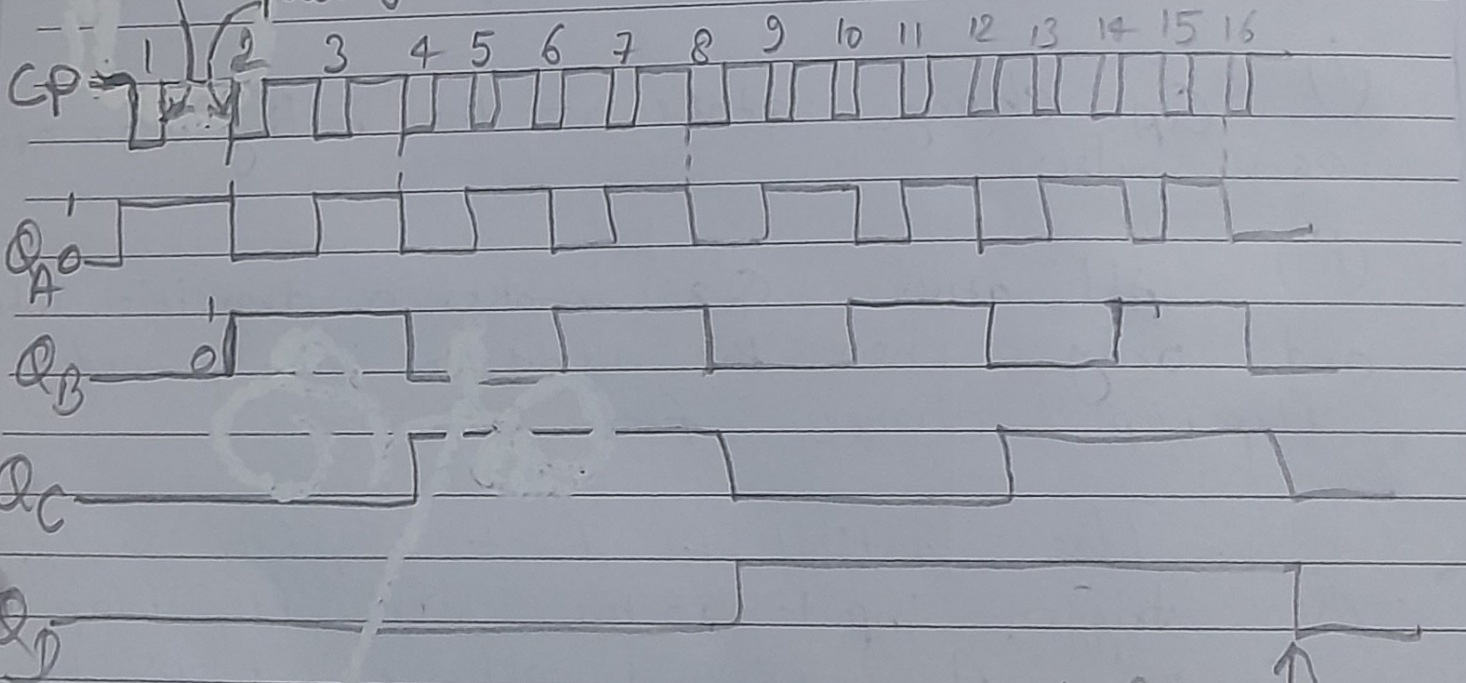
(i) Q_A change state at the falling edge of each pulse.

(ii) All other Q's make a transition when and only when the output of the preceding flip flop changes from 1 to 0.

The output of first flip flop acts as the trigger input to the next flip flop and so on. Assume that all flip flops have been cleared by a 1 on all C_D inputs. The fun^n of the chain

of flip-flops as to how their states change. i.e. their outputs become high (a 1) or low (a 0) can be described as follows, remembering that flip flops can change their state only at the falling edge of a CP:





All flip flops outputs are high after CP = 15

fig 1 (a) 4-bit ripple counter showing a count of 16 and 13.
(b) waveform of flip flop output.

Input Pulse	Flip flop outputs			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

For CP=13, $Q_A=1$, $Q_B=0$, $Q_C=1$, $Q_D=1$
All flip flop outputs go high after CP=15
When CP=16 arrives to respect A_1 all the others are also reset because of falling outputs

fig 1 (c) Table showing state of flip flops at each count.

(i) After one CP (say first CP):

After one CP, the output of A goes high ($Q_A=1$). It becomes high at the falling edge of first CP. The second flip flop will not be affected by the positive going edge of the first CP.

(i) When second, fourth and eighth CP arrives: At the falling edge of second CP, first flip flop, A_1 again changes its state so that $Q_A = 0$ (a low). Thus we get the falling edge of Q_A at which the second flip-flop B, will be triggered and then its output Q_B goes high (a 1). It will remain in this state until two more CP (numbered 3rd and 4th in fig 1(b) occur. This is because falling edge of Q_A will occur only at the arrival of fourth CP. At the falling edge of Q_A (the input of flip flop B) second flip-flop changes its state so that $Q_B = 0$ (fig 1.b).

But with $Q_B = 0$, we get the falling edge of Q_B at which the third flip flop, C will be triggered so that its output $Q_C = 1$. It will remain in this state until the arrival of eighth CP because falling edge of Q_B will occur only at the arrival of eighth CP. At the falling edge of Q_B, third flip-flop changes its state so that $Q_C = 0$ fig (1 b).

But with $Q_C = 0$, we get the falling edge of Q_C at which the fourth flip-flop D will be triggered so that its output goes high, i.e., $Q_D = 1$. It will remain in this state until the arrival

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of sixteenth CP because falling edge of Q_C will occur only at the arrival of sixteenth CP fig 1(b).

(iii) Arrival of sixteenth CP: After 15 clock pulses, all the flip-flop Q outputs are high (a 1). Thus when the sixteenth CP arrives to reset A, all other flip-flops are reset i.e. outputs Q_A, Q_B, Q_C and Q_D all go low (a 0). The circuit then starts to count once more. This is called a scale of 16 counter. fig 1(c) shows the state of the flip-flops at each count.